Amendments to the Specification

Kindly amend the specification as follows:

Page 1, between the title and the heading "**BACKGROUND OF THE INVENTION**", insert

--CROSS REFERENCE TO RELATED APPLICATIONS

This is a divisional application of application Serial No. 10/320,660, filed December 17, 2002, which is a divisional application of Serial No. 09/759,639 filed January 16, 2001, now U.S. Patent No. 6,528,854, which are hereby incorporated by reference in their entirety for all purposes.—

Please amend the title as follows:

SEMICONDUCTOR DEVICE ~~AND METHOD FOR MANUFACTURING THE SAME~~ HAVING THICK INSULATING LAYER UNDER GATE SIDE WALLS

Please replace the paragraph beginning on page 1, line 10 with the following amended paragraph:

This is a counterpart of, and claims priority to, Japanese Patent Application No. 2000-[[1250]] 010250, filed on Jan. 17, 2000, the contents of which are incorporated herein by reference.

Please replace the paragraph beginning on page 9, line 21 with the following amended paragraph::

A SiN sidewall layer, having a thickness from 100nm to 200nm, is formed on the semiconductor substrate using LP-CVD. An anisotropic etching technique, such as a RIE method, is employed to etch the SiN sidewall layer, so that SiN sidewalls 222 are formed as seen in Fig. 6(c) ~~fig. 6(c)~~. (Step 55) Subsequent steps are the same as those in the first embodiment. ([[Step]] Steps 56-58)

Please replace the paragraph beginning on page 10, line 26 with the following amended paragraph:

A SiN sidewall layer, having a thickness from 100nm to 200nm, is formed on the semiconductor substrate using LP-CVD. An anisotropic etching technique, such as a RIE method, is employed to etch the SiN sidewall layer, so that SiN sidewalls 322 are formed as seen in Fig. 9(b). (Step 84)

Please replace the paragraph beginning on page 14, line 1 with the following amended paragraph:

A SiN sidewall layer, having a thickness from 100nm to 200nm, is formed on the semiconductor substrate using LP-CVD. The formation of the SiN sidewall layer is performed at a temperature of over 850°C ~~Experiments os~~. In experiments, the ~~inventor~~ inventors have [[shwon]] shown that high temperature formation of the SiN

sidewall reduces the hydrogen that diffuses into the semiconductor substrate. An anisotropic etching technique, such as a RIE method, is employed to etch the SiN sidewall layer, so that SiN sidewalls 522 are formed. (Fig. 15(b), Step S144)

Please replace the paragraph beginning on page 17, line 17 with the following amended paragraph:

The gate electrode material 716 and the cap layer material 720 are formed on the gate oxide layer 724. A lithography method and an anisotropic etching technique, such as a RIE method, are employed to etch the gate electrode material [[616]] 716 and the cap layer material 720. The gate electrode [[616]] 716 and the cap layer are thereby formed. (Step S202)